# *Potentialities of common-used TDC chips for high-speed event timer design*

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# Introduction

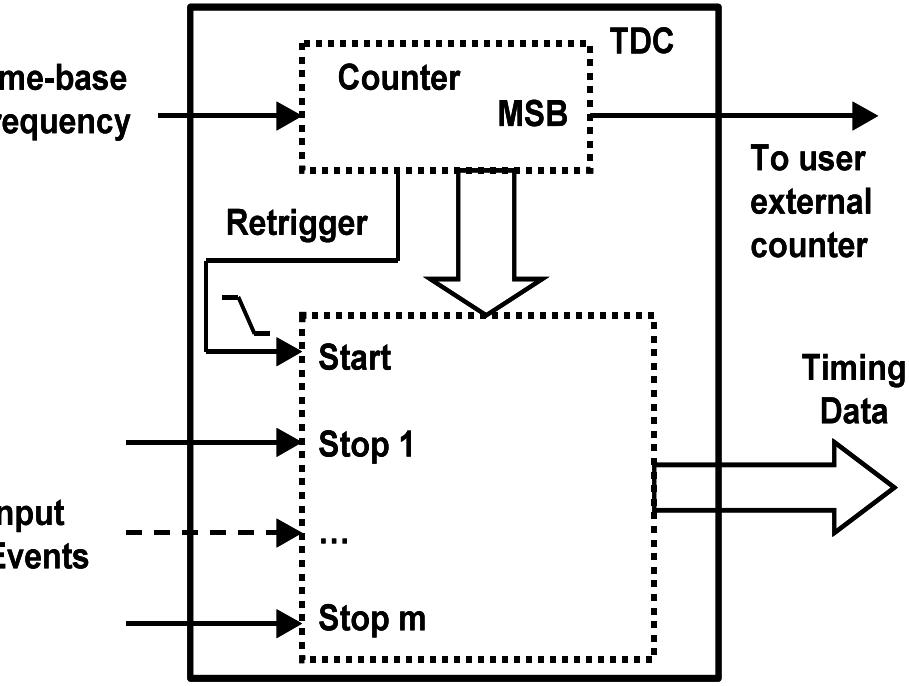
Basically commercially available TDC chips are not meant for continuous event timing. Nevertheless it is of interest to use their most attractive features (high speed, low power consumption, extended functionality, etc) for designing of true event timers.

In this report we consider potentialities and actual performance of high-speed Event Timer based on application of high-performance TDC-GPX from Acam-messelectronic Gmbh.

# The main problem to be solved

**The main drawback of typical TDC chips is that they are implemented according to the traditional time interval measurement technique and have a limited time interval measurement range. It means that they cannot be used directly to build true Event Timers.**

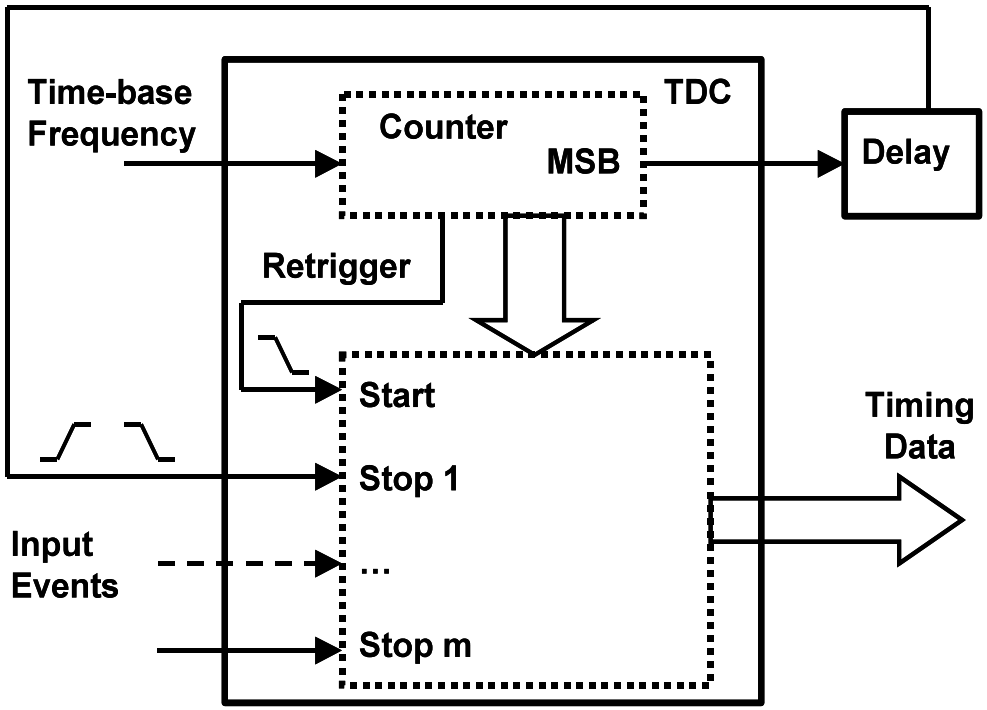
TDC-GPX has additional restarting circuitry internally allowing the measurement range extension up to 1.28 ms but not more.




The offered by the manufacturer simple way to extend the measurement range by an external counter can not be easily realized due to the problems with correct data reading at high event rates.

## What has been done by us?

# Marker event insertion circuitry for time scale extension

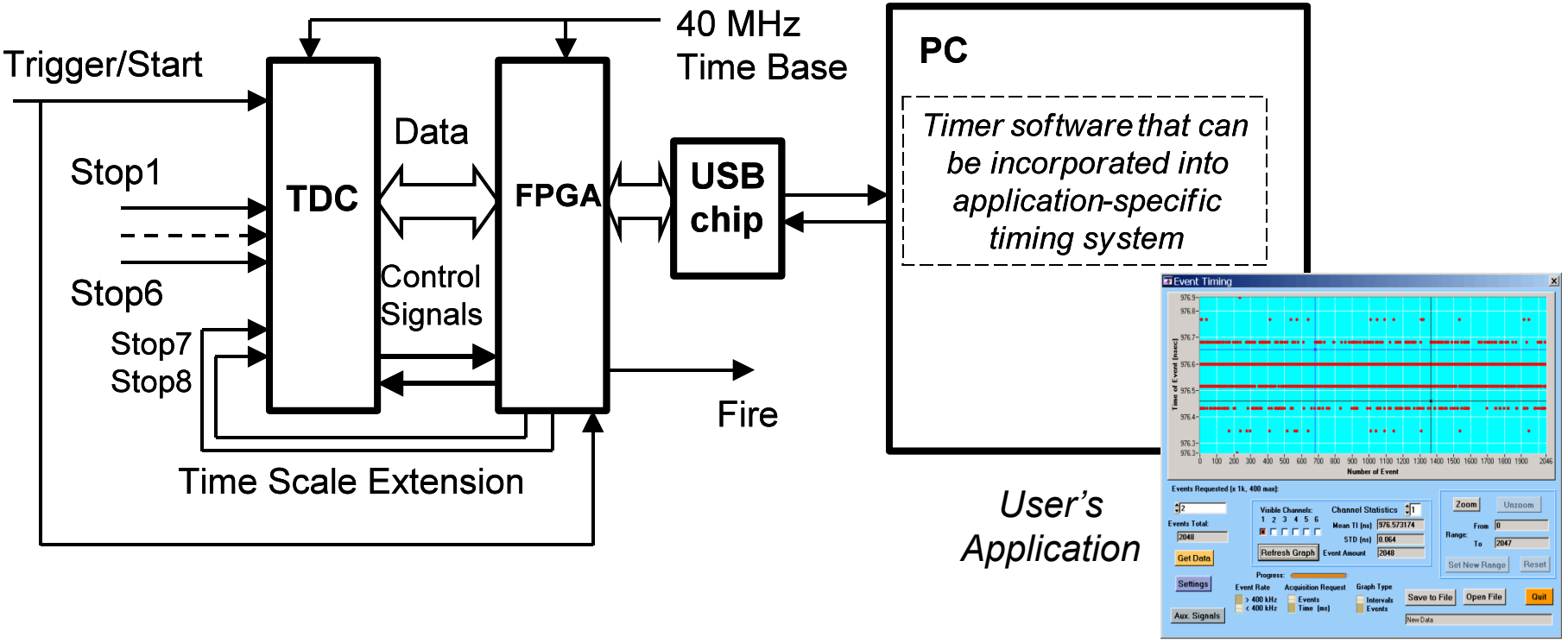



One measurement input of the TDC is assigned as a specific marker input. The MSB of the restart counter is delayed and then is fed into this input. The marker input is configured for accepting both positive and negative edges. In this way we insert specific marker events into the output digital data stream.

The following constructing of single-valued time scale could be done either by the controller block firmware or by PC software where the data finally come in most of applications. The firmware or software detects the marker measurement data blocks and constructs the extension time scale simply as a variable to use for composing resultant time stamps.

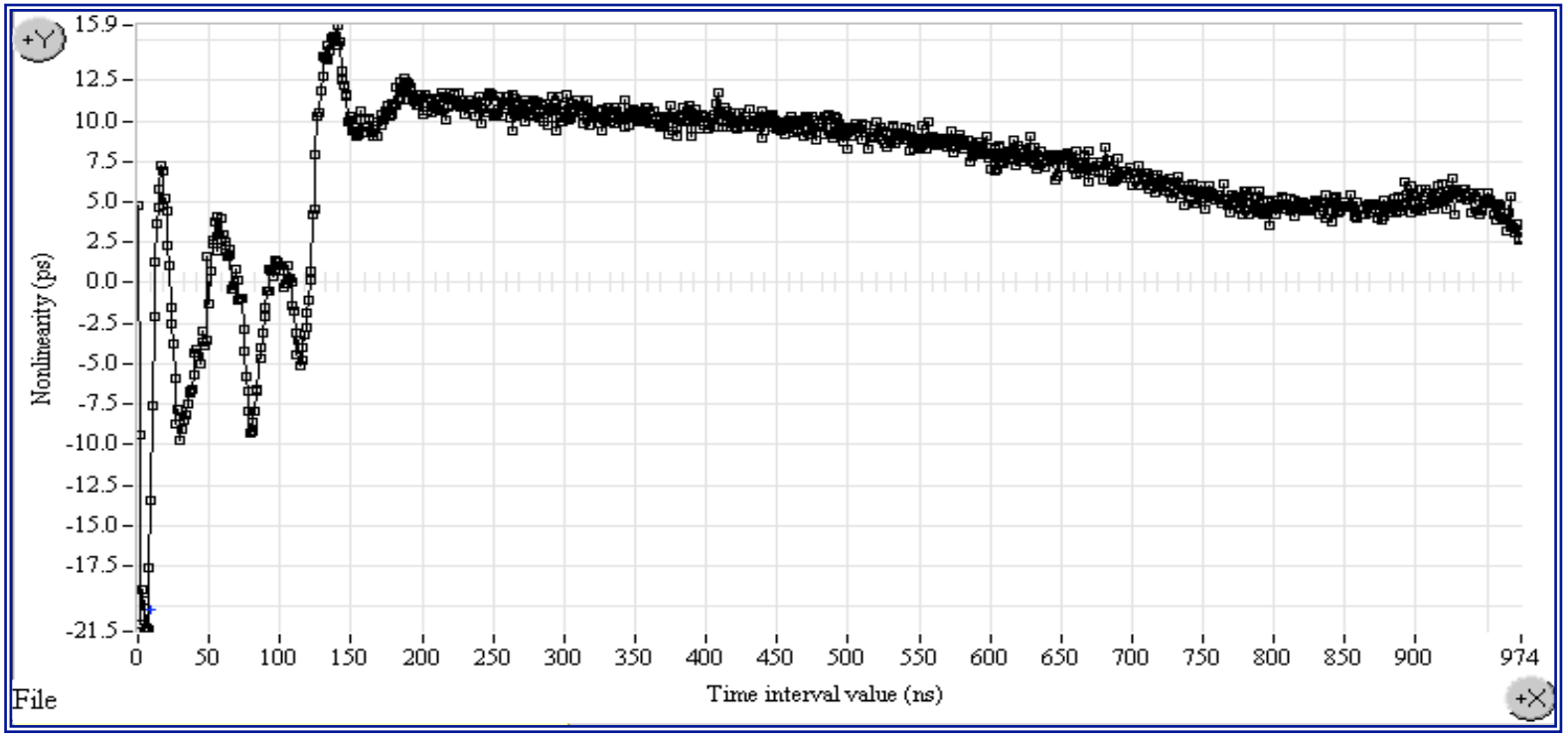
# Event timer implementation

**Research has resulted in a pilot model of high-speed event timer (HSET) with unlimited range of time measurement.**

# Evaluation of HSET characteristics

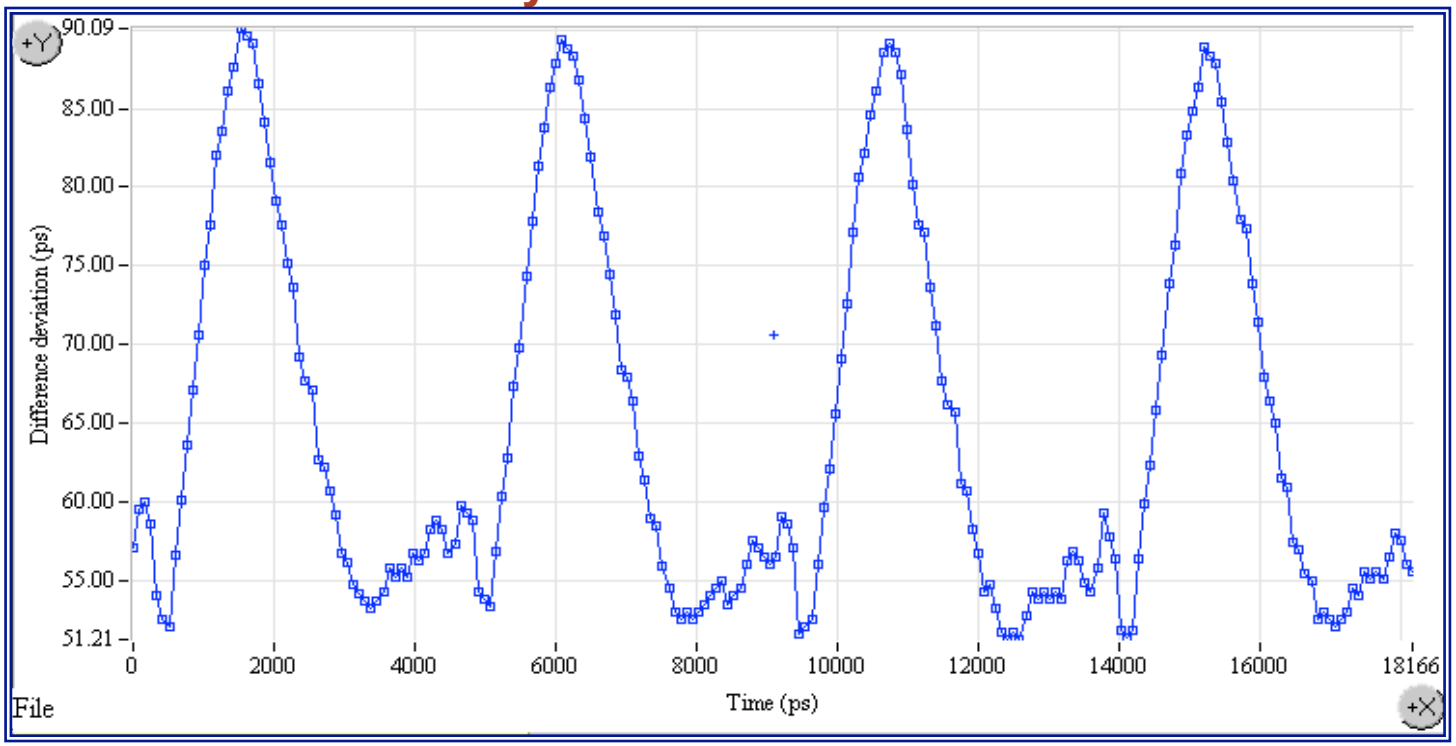
## Non-linearity in time interval measurement between adjacent events




**There are noticeable non-linearity errors in the beginning of time interval range caused mainly by cross-talk between input channels. After 150-200 ns of time intervals the non-linearity errors become negligible small.**

# Evaluation of HSET characteristics

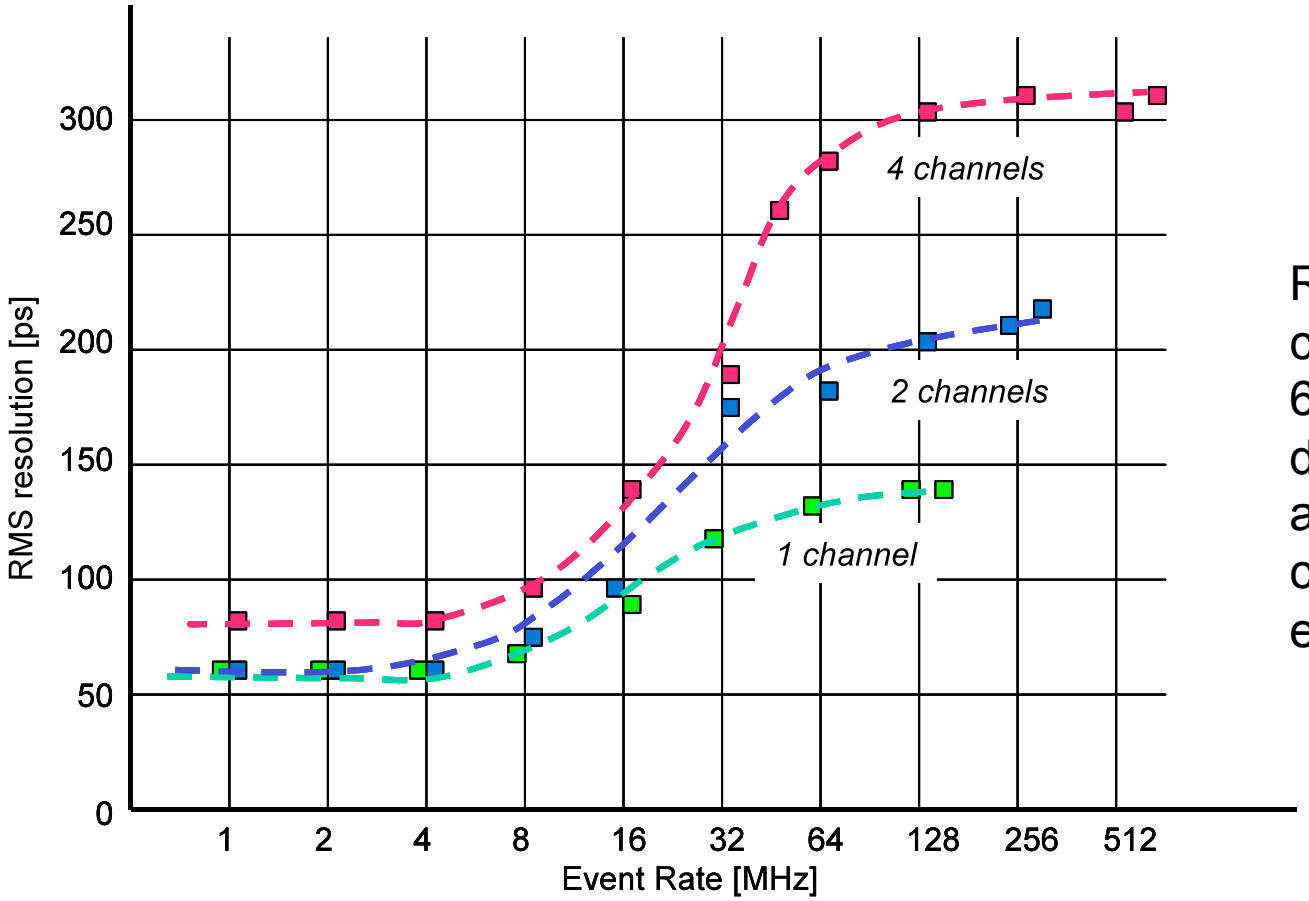
## Nonlinearity in event time measurement




**The graph reflects the nonlinearity of the TDC's discrete interpolator over 4 periods of its operation.**

# Evaluation of HSET characteristics

## RMS resolution vs. aggregate input event rate




RMS resolution considerably varies from 60 ps to 310 ps depending on the amount of emploied channels and aggregate event rate.

**The main reason of the resolution degradation is the on-chip PLL performance degradation caused by internally induced noises**

# HSET features


- 6 independent event measurement channels
  (4 primary channels and 2 TAG channels)
- 90 ps typical RMS resolution (at event rate up to 5 MHz)
- 6.5 ns dead time (each channel),
- No limitations for different channels, rising/falling edges accepted
- Limitless measurement range
- Up to 150 MHz burst rate (each channel, up to 32 events in one burst)
- Up to 2.5K-event bursts at 40 MHz aggregate for all channels
- Average measurement rate (aggregate for all channels) – 5M-events/s
- Triggering – external (rising or falling edge) or internal (from the PC)
- Programmable thresholds for input signals (+/- 1.25V with 0.6mV step)
- 2 independent internal programmable gates – from 0 ns to 419 ms, step 25 ns
- Internal time base 40 MHz with long term stability +/- 0.5 ppm
- Accepts an external 10 MHz reference signal, onboard low jitter PLL
- Fire (stimulus) generator with the period range from 1 μsec to 1678 ms (step 0.1 μs)

# Conclusions

Generally it can be concluded that some of currently available commercial TDC chips (such as TDC-GPX) are applicable for event timer designs that target the applications where compact implementation and high rate of multi-channel event timing are mostly needed.

As for the achievable resolution, it is not up to the mark (especially at very high event rates); the existing limitations are caused by imperfectness of TDC-chip realization. It seems that a custom design of a TDC chip, specifically tailored for building the true event timers (in cooperation with a manufacturer), may lead to much better results.

The event timer (HSET) designed in the framework of the presented research offers a good price/performance ratio as compared to the commercially available devices of such kind. We hope that this can make it (or its options) attractive for the applications related to Laser Ranging.